Effects of surface plasma treatment on threshold voltage hysteresis and instability in metal-insulator-semiconductor (MIS) AlGaN/GaN heterostructure HEMTs

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Abstract: In a bid to understand the commonly observed hysteresis in the threshold voltage in MISHEMTs during gate forward bias stress, we analyzed a series of measurements on samples with no pretreatment and with two different plasma pretreatments. The observed changes is quasi-equilibrium threshold voltage (V_{TH}), forward bias related V_{TH} hysteresis and electrical response to reverse bias stress required the use of a disorder induced gap state (DIGS) model combined with a discrete level donor at the dielectric/semiconductor interface. TCAD modelling was carried out which demonstrated the possible differences in the interface state distributions to explain the observations consistently.

Introduction

In recent years, GaN based AlGaN/GaN high electron mobility transistors (HEMTs) have demonstrated excellent potential for both RF and power electronics applications owing to very favorable material characteristics such as high 2DEG mobility and concentration and a wide band gap to support a large blocking voltage. Metal-insulator-semiconductor (MIS) structures are often preferred over Schottky gate structures in power electronics applications because of their ability to suppress the gate leakage current, engineer the threshold voltage for both depletion and enhancement mode operation, enhance the device capability to withstand larger gate voltage swing and to improve the gate-drain breakdown voltage [1-3].

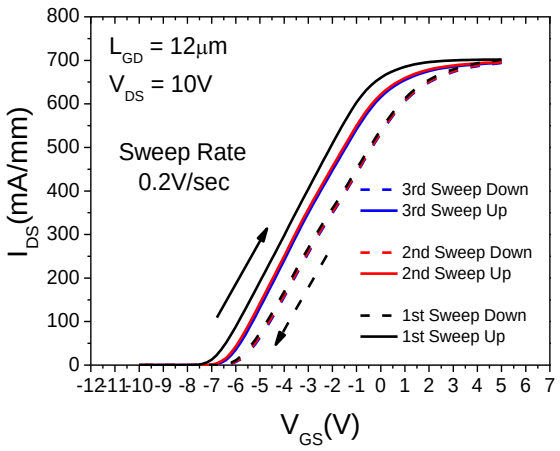
There have been several successful demonstrations of using various gate dielectric layers by different deposition techniques [4-11] to achieve the aforementioned objectives in AlGaN/GaN HEMTs. However, introducing a gate dielectric layer inserts an additional, likely non-ideal, interface in the structure which can result in charge trapping/de-trapping effects associated with the dielectric/III-nitride interface and/or the bulk dielectric itself. The dynamic charging and discharging process of these traps can affect the stability of the threshold voltage causing significant variations in switching performance. The effects can be observed through threshold voltage hysteresis in bi-directional gate transfer sweeps from below threshold to high forward bias and back again [12-17]. Previously, dynamic processes have been studied in detail using CV dispersion measurements as a function of frequency and temperature [18] and stress recovery analysis in HEMTs by monitoring the threshold voltage (V_{TH}) after forward gate bias [14-25]. These studies have yielded a broad distribution of stress and recovery time constants, suggesting a wide distribution of traps both at the interface and within the AlGaN barrier [16]. However, attempts at directly comparing different surface preparations before the dielectric deposition have been limited [26]. Also, in power switching applications, GaN HEMTs are required to block large voltages in the pinched-off state and any threshold voltage instability in such situations can be a serious concern. There are a few reports on the influence of negative gate bias stress on the threshold voltage in recessed barrier AlGaN/GaN MISHEMTs [27] and MOS GaN FETs [28-29] but there has been no comparisons highlighting the differences between surface preparations and no attempts at consistency between forward and reverse stress models.

In terms of mitigation of these unwanted dynamic effects, using a $NH_3/Ar/N_2$ or N_2 plasma to achieve surface nitridation [18,19,30,31] and oxygen plasma treatment [20] prior to dielectric deposition have been shown to be effective. In most of this past work the focus has been on understanding the dynamic mechanisms leading to drift and/or hysteresis in V_{TH}. In practical device operation the quasi-equilibrium value and stability of V_{TH}, as well as its dynamical responses, are important and the effects of surface treatment prior to dielectric deposition are crucial to minimise these effects. There is no standard for stress magnitudes and times, which make it difficult to compare publications across the literature and direct comparison of different surface preparations on the same samples using a wide range of probing techniques are lacking and consistency between all observations has still not been reported.

In this work, we have used aluminum oxide (Al_2O_3) as a gate dielectric in AlGaN/GaN MISHEMTs because of its wide band gap (7-9eV), large conduction band offset (2.16eV), high breakdown field (>10MV/cm) and dielectric constant (8-10) [13]. We have performed *in-situ* nitrogen (N_2) and argon (Ar) plasma treatments before atomic layer deposition (ALD) of Al_2O_3 in an attempt to understand the role of both the plasma and its chemical nature. In the past, *in-situ* N_2 plasma [18,19,30,31] and Ar plasma treatment [21] were studied separately. Here we have compared *in-situ* N_2 and Ar plasma treatments on depletion mode AlGaN/GaN MISHEMTs before the deposition of 20nm Al_2O_3 dielectric using ALD and carried out positive and negative gate bias stress measurements to evaluate the stability of the threshold voltage. We have studied the effects of high forward gate overdrive, negative gate bias stress and the shift in the quasi-equilibrium V_{TH}. We propose a model to link and explain all these observations which has not been attempted in the past.

Results and Discussion

The wafers were grown by Metal Organic Chemical Vapor Deposition (MOCVD) on 6-inch Si substrates. To facilitate the growth on Si, a nucleation layer of AlN (250nm) was used together with a series of compositionally graded carbon doped AlGaN and GaN layers. A 1 nm mobility enhancement AlN layer was grown on the channel layer and an $Al_{0.28}Ga_{0.78}N$ barrier layer of thickness 27nm grown on top of that. Finally, the wafer was capped with a 2nm undoped GaN layer. A standard device fabrication procedure was followed with mesa isolation achieved by a chlorine-based recipe in an inductively coupled plasma etching chamber. The ohmic contacts used Ti/Al/Ni/Au (20nm/120nm/20nm/45nm) metal stacks which were annealed at 850^0C for 30 seconds. After ohmic contact formation, a standard 100nm SiO_2 layer was deposited using the plasma enhanced chemical vapor deposition (PECVD) technique. A 1.5μm gate window was etched through the SiO_2 layer. Before the 20nm Al_2O_3 gate dielectric atomic layer deposition, *in-situ* 150W N_2 plasma or 50W Ar plasma treatment for 5 minutes was performed on the samples and one sample was prepared without any pre-treatment to serve as the reference sample. After dielectric depositions, forming gas annealing (FGA) was performed in N_2 and H gas ambient at 430^0C for 30 minutes. Then T-shape gates with 1μm gate field plates were defined using a standard Ni/Au (20nm/180nm) metal stack. Finally, bond pads using Ti/Au (20nm/200nm) were formed via etches through the dielectric layers. Hall measurements yielded a mobility of 1909 $cm^2V^{-1}s^{-1}$ and 2DEG density of $8.7\times10^{12}cm^{-2}$.



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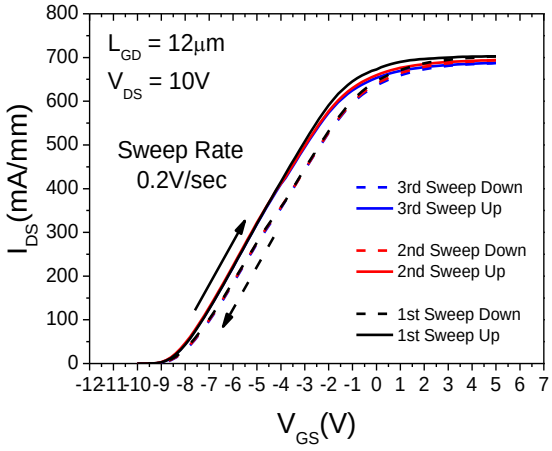

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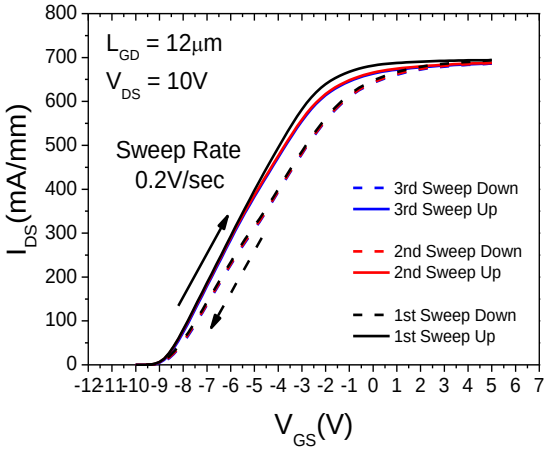


(c)

Figure 1. The gate transfer characteristics of AlGaN/GaN MISHEMT before (a) and after (b) 150W N_2 and (c) 50W Ar plasma pre-treatment.

The gate transfer characteristics of AlGaN/GaN MISHEMT devices with and without *in-situ* N_2 and Ar plasma pre-treatment before the 20nm Al_2O_3 deposition are shown in figure 1. Starting from the virgin device, the gate transfer sweep is performed from -10V to +5V V_{GS} upward and then backward from +5V to -10V V_{GS} with V_{DS} kept at 10V. This bi-sweep is repeated three times. It can be seen from figure 1 (a) that, in the reference sample after the first upward sweep, there is a positive shift in the threshold voltage compared with the second upward sweep and a considerable hysteresis (~1.2V) in the threshold voltage. This is attributed to trapped electrons at the interface between the dielectric and III/nitride semiconductor and/or bulk dielectric traps when the gate is sufficiently positive biased to facilitate electron transfer from the 2DEG. Once the electrons are trapped they are slow to emit and travel to the channel when the positive gate bias is removed. This gives rise to a time dependent positive shift in the threshold voltage or hysteresis. Regardless of the quasi-equilibrium threshold voltage the transferred charge injected into the dielectric interface is related to the voltage only, since the forward bias capacitance is just that due to the dielectric once electron transfer occurs, as indicated by the loss of gate control (figure 1). The origin of the interface traps can be due to the presence of a poor quality native oxide layer formed on the semiconductor surface, dangling bonds or interface impurities. In the N_2 and Ar plasma treatment samples in figure 1 (b) and (c) the shift in the threshold voltage between the first and subsequent sweeps and hysteresis, measured at the mid current point, is reduced (ΔV_{TH} from 1.2V (reference) to 0.2V in the N_2 and 0.25V in the Ar plasma treated sample). In addition, there is also a negative shift in the quasi-equilibrium threshold voltage (allowed to stabilize over several days) of about ~1.5 to 2V after both plasma pre-treatments.

Hysteresis

Considering the hysteresis first, the corresponding reduction in the hysteresis voltage on the plasma treated samples compared to the untreated samples under the same bias sweep conditions indicates either a reduction in the number of trapped electrons and/or changes to the capture/emission dynamics. To test for a change in the number of trapped electrons due to the treatment, we performed hysteresis measurements as a function of forward gate bias, keeping the forward bias duration constant. Figure 2 shows the hysteresis increasing systematically with the increase in positive gate bias voltage up to +10V V_{GS} for all samples. The lack of saturation of the hysteresis voltage with increasing bias indicates the number of interface traps exceeds the electron charge resulting from the forward gate bias for the range of biases and samples considered. Any net reduction in the number of interfacial traps due the plasma

treatment would have little effect under these conditions, provided the trap numbers still dominate. Note, however, that the slopes of the linear portion of theses curves (V_{GS} below ~8 V) are different for the plasma and untreated samples. For hysteresis measurement times much less than the emission times of the trapped electrons, the slopes should be related to the oxide geometric capacitance which is fixed. Hence, the lack of a common slope confirms a decrease in the trapped electron emission times as a result of the plasma treatment. This observation is reinforced by the tapering of the hysteresis voltage observed near the end of the measurement in the treated samples which indicates significant emission of trapped electrons during the full measurement time (~25 s). However, the emission pathway for electrons from the interface to the 2DEG channel through the AlGaN barrier is expected to be unchanged between the treated and untreated samples. A possible reason for the decreased emission time could be that a greater proportion of trapped electrons occur near the conduction band of the barrier, enabling these electrons to more easily emit into the conduction band or gain an energy advantage during the hopping transport through the barrier (further explanation later). Over the range of devices measured, the N_2 plasma treated sample showed only marginally improved hysteresis compared to the Ar plasma treated sample, indicating perhaps that nitridation [18,19,30,31] in not important under these conditions.

We next look at the effects of increasing the gate forward bias stress time. Figure 3 (a) and (b) shows the positive threshold shift with forward bias stress time and the measurement sequence respectively. The devices are de-stressed with negative gate bias to restore the initial threshold voltage and the experiment is repeated with increasing gate stress time. The gate transfer sweep used to measure the shift in threshold voltage takes about 25 seconds to complete, at which time some relaxation of the trapped charge will occur, resulting in a reduction in the measured threshold voltage shift over that immediately after the forward bias stress. Despite this, the data of Figure 3 indicates two distinct charging mechanisms. These can be explained by a rapid occupation of interfacial traps occurring initially, followed by a much slower tunneling to traps within the dielectric [14-17]. The observed (slower) timescale for the tunneling into the dielectric is similar for all three samples, as expected since the pretreatment will not affect the bulk properties of the dielectric. The data is also consistent with the notion that the pretreatment increases the speed of relaxation of the charge from the interface to the 2DEG where the faster plasma treated samples show a reduced shift in threshold voltage during the hysteresis measurement.

To gain a better understanding of the hysteresis-related relaxation process, continuous recovery times in response to forward gate bias were measured and are shown in figure 4. The device drain current was first measured with no gate bias and V_{DS} = 1V to serve as a reference. V_{DS} was limited to 1 V in this setup to avoid influence due to heating effects. The devices are then subjected to a high positive gate overdrive condition (V_{GS} = +7V, V_{DS} = 0V) for 1 sec. The duration for the positive gate overdrive of 1 sec was chosen to limit the electron charge trapping to within the semiconductor/dielectric interface and avoid charge spillover as much as possible to the slower emitting bulk dielectric traps. After the forward gate overdrive, the devices are biased back to V_{GS} = 0V and V_{DS} = 1V and the drain current, which reflects the changes in the 2DEG charge due to trapping in the semiconductor/dielectric interface, is measured over a period of 10 hours with a 200 msec sampling rate. The ratio of drain current before and after the gate overdrive and experimental test sequence is shown in figure 4(a) and (b) respectively. The variations in the drain current reflect the variations in trapped charge under the gate. Due to the rapid sampling of the relaxation process this method [14] greatly reduces inaccuracies in the measured threshold drift. However, significant relaxation may occur for all curves within the first measurement time period (0-200 ms) [14] and the initial relaxation characteristics therefore cannot be resolved. For the same bias voltage, the trapped charge at the instant of the removal of the bias would be the same and hence, in this case, the plasma treated samples appear to relax more quickly compared to the untreated sample during this initial period, in line with the differences in hysteresis. The prolonged recovery times indicates that threshold voltage instabilities can cause difficulties over a wide range of switching conditions in practical systems.

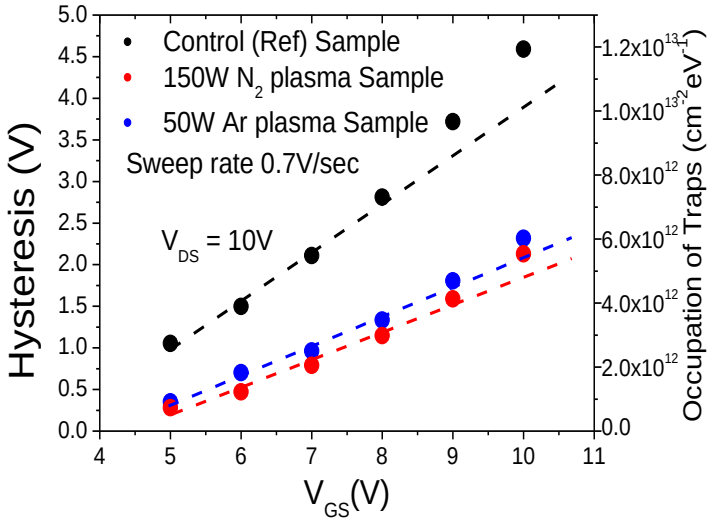
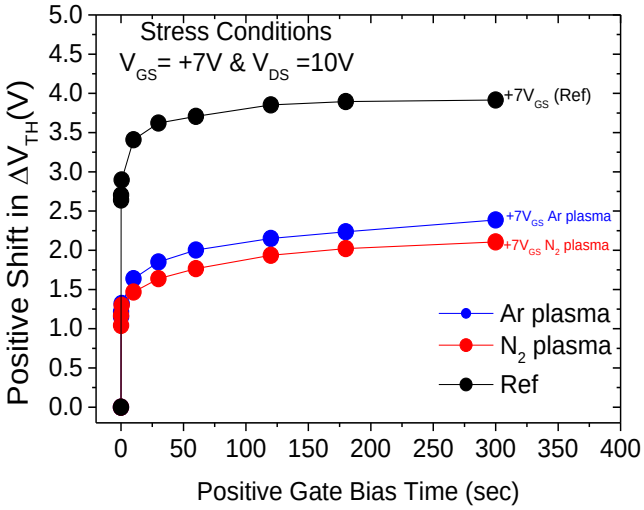


Figure 2. The built up of hysteresis with increase in the positive gate bias voltage and estimated occupation of trapped charge.



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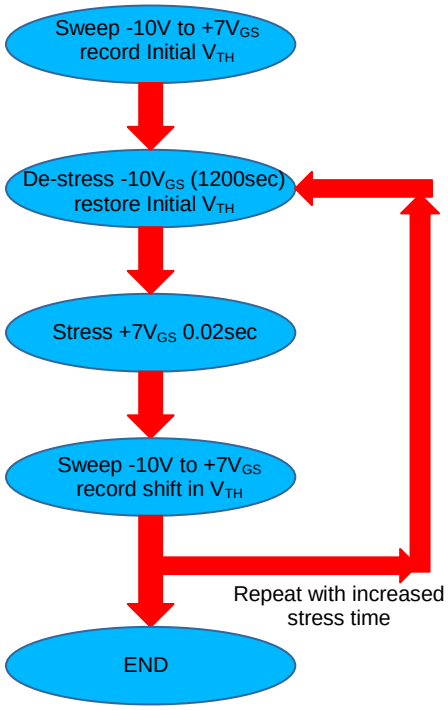

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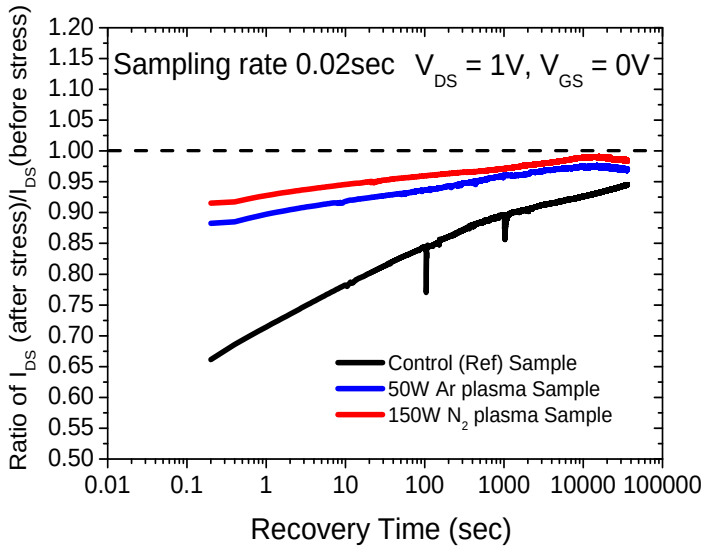
Figure 3. (a) The positive shift in threshold voltage with positive gate bias stress time (b) experimental test sequence.



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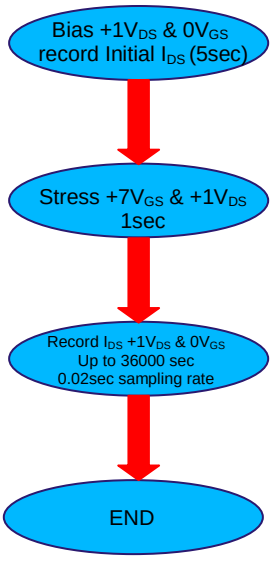

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Figure 4. (a) The drain current recovery time after 1sec +7V_{GS} stress in reference and plasma treated samples (b) experimental test sequence.

Reverse Bias Stress

Power devices are often required to withstand large blocking voltages in the pinched-off state and any threshold voltage shift in such situations can be problematic. There are a few reports of negative gate bias stress in recessed barrier AlGaN/GaN MISHEMTs and MOS structure GaN FETs [26-28]. However, there has been no comparison between different surface preparation methods and no attempt at correlation with forward bias stress results. In this work, we have performed negative gate bias stress on conventional AlGaN/GaN MISHEMT devices both with and without plasma pre-treatment to evaluate the stability of threshold voltage in such scenarios and gain some further insight into the differences between pretreated and untreated samples.

The negative shift in the threshold voltage of AlGaN/GaN MISHEMTs with negative gate bias stress time using -5V and -10V V_{GS} is shown in figure 5 (a) along with the experimental sequence (b). In this experiment, virgin devices are initially swept from -10V to 0V V_{GS} to record the initial threshold voltage and then negative gate bias stress is applied with -5V or -10V V_{GS} for 0.02 seconds after that, devices are swept from -10V to 0V V_{GS} to record the shift in the threshold voltage. The experiment is then repeated with increased negative gate bias stress time.

Figure 5 (a) shows the shift in the threshold voltage as a function of stress time, which is due to the transport of electrons from the dielectric/barrier interface towards the channel. The shift is considerably greater in the reference sample compared to the plasma-pretreated samples. Contrary to the results for positive gate bias stress, the charge adjustment under negative stress is much slower than the measurement time, giving a reduced error in sampling the threshold shift. The difference between the reference and N_2 and Ar plasma treated samples after one hour stress time is ~1.7 V, which is similar to the observed quasi-equilibrium threshold voltage differences (figure 1). This is most likely due to the differences in stored charge close to the quasi-equilibrium Fermi level which gives rise to the differences in the quasi-equilibrium V_{TH} (further explanation later).

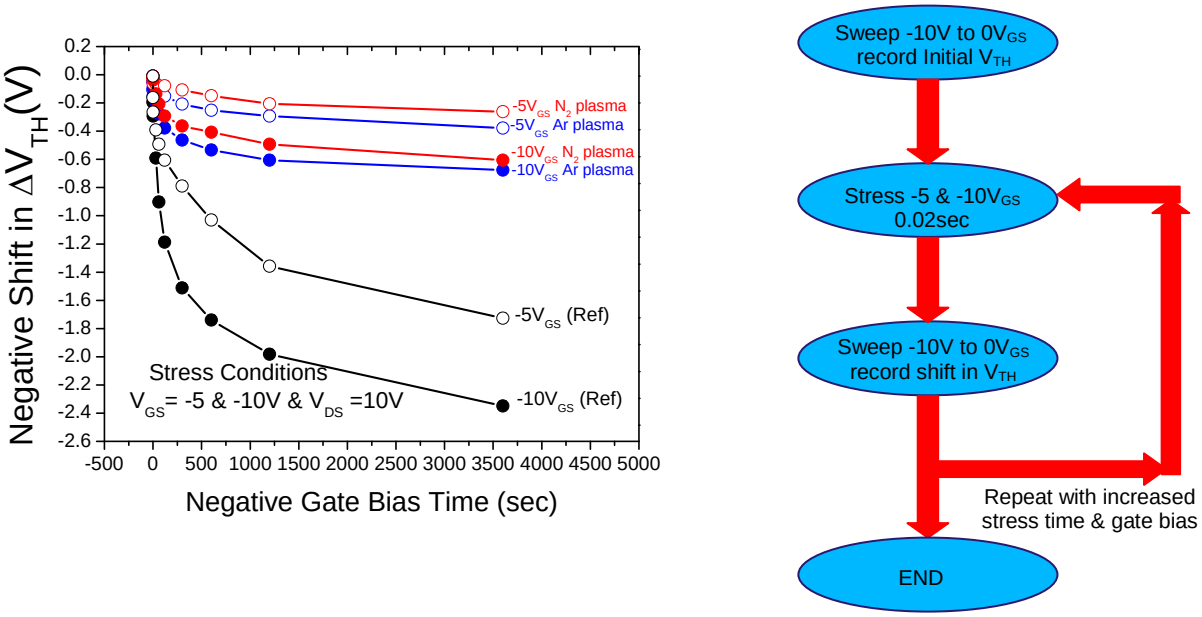

Figure 5. (a) The negative shift in threshold voltage with negative gate bias stress, and (b) experimental sequence with negative gate bias stress.

Model and Discussion

To date, the origin of the 2DEG charge in AlGaN/GaN heterostructures is still a conundrum. Although it is widely accepted that the surface and interface states (in MIS structures) play a vital role, the exact nature of these interface states and their distribution within the forbidden gap is still under debate. The various models were summarized and discussed by Bakeroot et al [32]. Each model has its own limitations but may explain behavior within limited specific conditions.

The unified disorder induced gap states (DIGS) model [33,34] has often been utilised to explain different V_{TH} hysteresis behavior. This model divides the U-shaped interface state density into donor- and acceptor-like states separated by the charge neutrality level (E_{CNL}) [33] with the Fermi level (E_F) close by (figure 6(a)) . Although the DIGS model can explain the formation of the 2DEG, some additional discrete donor-like interface states, particularly those which have been associated with nitrogen vacancies [35], may still be needed to explain the 2DEG variation with barrier thickness and composition, and to place E_F above E_{CNL} [32, 35]. The latter is a requirement for our model. Therefore, to help establish the charge details at the interface as a result of the plasma pretreatments, we used SENTAURUS TCAD to simulate a DIGS model together with discrete donor states associated with nitrogen vacancies, 0.37eV below the

conduction band [35], to explain our three main experimental observations after plasma pretreatment. These are 1) the negative shift in the quasi-equilibrium V_{TH} (~2V), 2) the faster emission rates (reduced hysteresis) and 3) the reduced negative shift in the V_{TH} during negative gate bias stress.

Figure 6 (a) shows the distribution of interface states along with the energy levels used in the SENTAURUS simulation to represent the plasma pretreated and reference (higher interface state density) samples. Note that the number of discrete donors and the magnitude of the DIGS distribution was chosen to yield the experimental 2DEG concentrations. The discrete donors are necessary to place the Fermi level above E_{CNL} but should not be large enough in number to pin the Fermi level at that level. However, many concentration combinations of DIGS and discreet donor levels will give the correct value of the 2DEG. Here we are mostly interested in the relative values of the DIGS density to model the observed electrical differences between the samples. The conduction band diagram at V_{GS} = 0 V (equilibrium state) for both samples is also shown in figure 6 (b). Note the small differences in the Fermi level position with respect to the conduction band. We excluded the 1nm AlN mobility enhancement layer in our model since it is unlikely to make any significant difference to our explanation. An E_{CNL} value of 1.78eV, as calculated by Mönch [36], was used. Due to the presence of the discrete donor states, the Fermi level position is slightly above the E_{CNL} level and donor-like states below the E_{CNL} level are considered frozen or fixed, i.e. they remained neutral (occupied) throughout, under all bias conditions considered [34]. The rationale for this assumption is that the time constants associated with states below mid band gap in AlGaN can be very large (10^{12} – 10^{20} sec) [34] and therefore are unlikely to change charge state in the gate transfer measurements. This is also borne out by the medium term stability of the pinch-off condition in normal HEMT operation.

The 2DEG charge per unit area, n_s, formed as a result of this model is given by

$$n_s = N_D^+ - N_A^- \qquad (1)$$

where N_D^+ the ionized donor density per unit area (here assigned to nitrogen vacancies) and N_A^- is the occupied acceptor-like state density below the Fermi level. To explain the observations we assume that the plasma pretreatment reduces the density of the U-shaped distribution of interface states, and hence the number of negatively charged acceptor states below the Fermi level, N_A^-, is reduced. Whilst the shift in n_s and hence the quasi-equilibrium V_{TH} after the plasma pretreatment can also be explained by simply

increasing the discrete donor states in equation 1, the explanation of the hysteresis and reverse bias observations require changes in the acceptor-like state densities [32, 34].

Figure 6 (c) shows the modelled results as described above compared with the experimental transfer characteristics for the reference and plasma pretreated samples. Reasonable agreement is obtained. In our model the ~2V shift in the quasi-equilibrium V_{TH} after plasma pretreatment is the manifestation of the reduced DIGS acceptor states density, N_A^-, in equation 1. The conduction band diagram of the reference sample under 0 V (equilibrium) and -10 V V_{GS} showing the charge transfer mechanism is shown in figure 7. In the equilibrium condition (0 V V_{GS}), occupied acceptor states are below the Fermi level and, as the gate is swept to reverse bias (-10 V_{GS}), these acceptor states are lifted above the Fermi level. However, the emission time constants of electrons in these acceptor states are such that they are unable to emit during the gate transfer sweep and so behave as fixed negative states in the reference sample. The presence of these additional acceptor states over and above those in the plasma treated samples results in the ~2V V_{TH} difference. When the negative gate bias is applied for a long enough time such as in the reverse bias stress measurements of figure 5(a), then the electrons in these acceptor states are eventually able to reach the 2DEG channel as shown in figure 5(a) via hopping through the AlGaN barrier traps and/or emission into the barrier conduction band. After nearly one hour negative gate bias stress (-10V_{GS}) the V_{TH} difference between the reference and plasma pretreated sample is ~2V as seen in the figure 5(a) which is equal to the difference in the equilibrium V_{TH}, reflecting the extra charge transfer in the non-treated samples. As stated previously, the donor-like states below E_{CNL} are considered too slow to take part in the reverse bias transients.

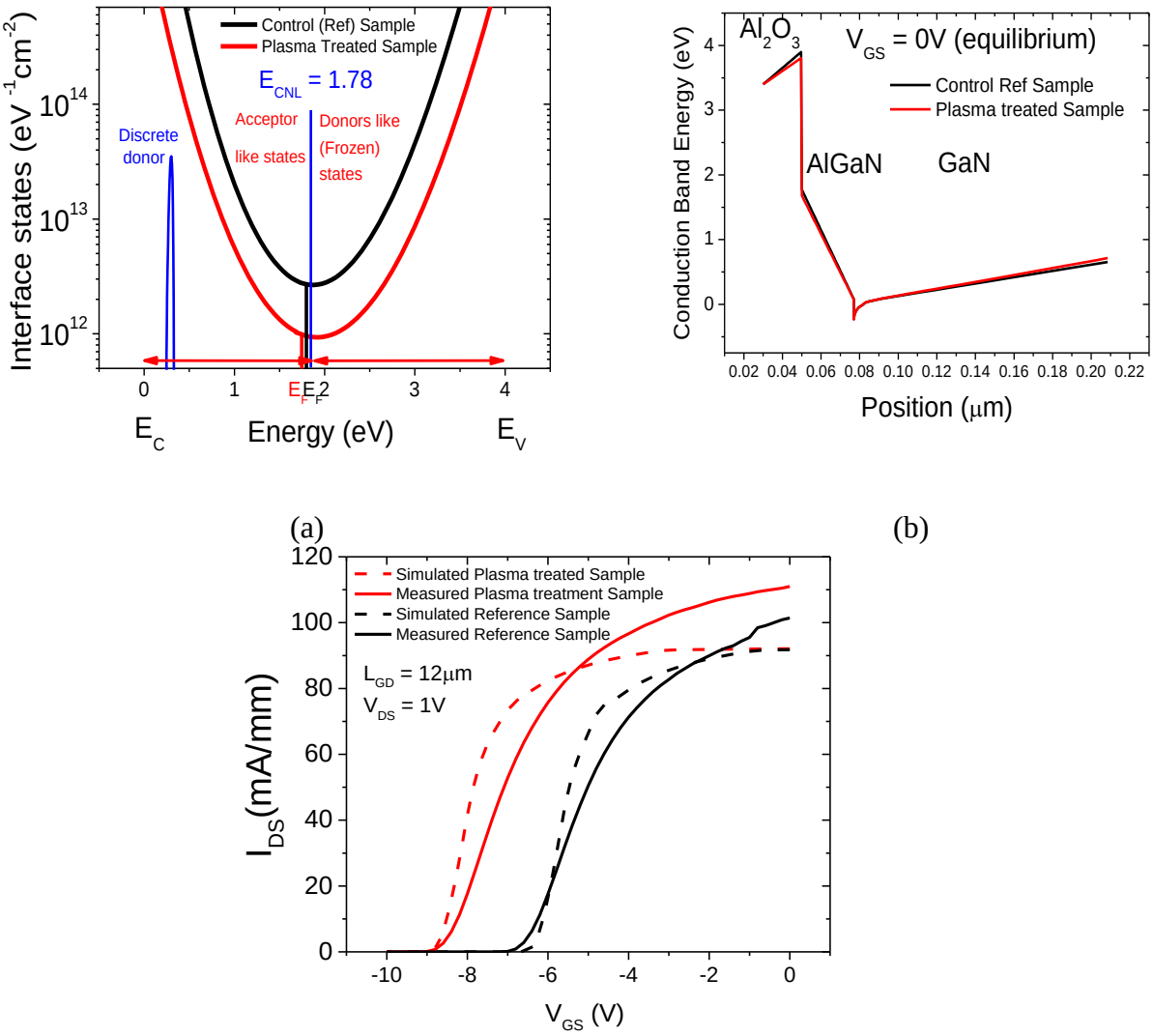

Figure 6. (a) The distribution of interface states used in the model of the reference and plasma treated samples. (b) Modelled conduction band diagram at equilibrium state in reference and plasma treated sample (c) Modelled and measured gate transfer sweep of reference and plasma treated sample.

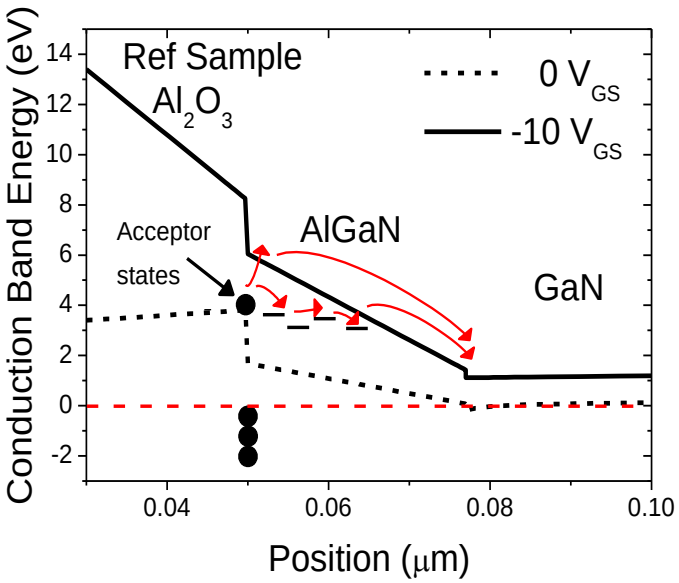

Figure 7. Conduction band diagram of reference sample at 0 and -10V_{GS} showing the electron transfer mechanism.

When the gate is sufficiently forward biased, the acceptor-like states above the Fermi level are filled with electrons and are responsible for the V_{TH} hysteresis in bi-directional gate transfer sweeps (figure 1). Under the forward bias condition, to trap the same amount of charge (fixed forward bias voltage) more states closer to the conduction band would get filled in the plasma pretreated sample compared to the reference sample, as shown by the red and black shading in figure 8. This difference in the occupation distribution of interface acceptor-like states can lead to faster electron emission in the plasma pretreated sample and reduced hysteresis.

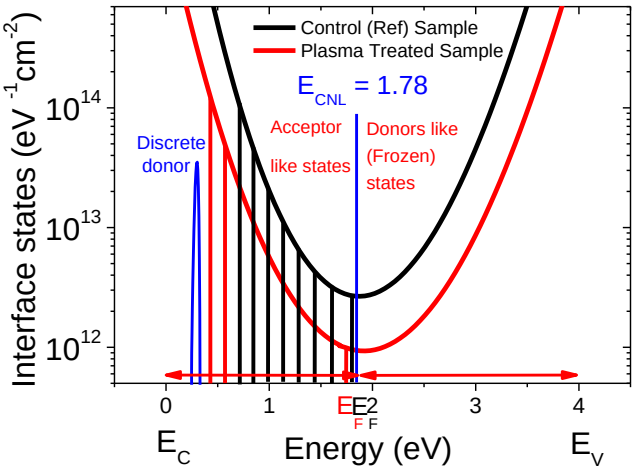

Figure 8. Filling of acceptor like states in reference (black lines) and plasma treated sample (red lines) to accommodate same amount of charge (7V) under the forward gate bias stress condition.

Surface Study

To understand the possible chemical changes on the surface after both plasma pretreatments, we performed X-Ray photoelectron spectroscopy (XPS) with 2.5nm Al_2O_3 dielectric layer thickness on both untreated and plasma pretreated GaN. Both plasma pretreatments reduced the O-C peaks equally which were previously reported to be detrimental to device performance [30]. In addition, the N_2 treated sample increases the Al-N bonding ratios which suggests a possible nitridation effect. There is also an increase in the Al-OH bond ratio after N_2 plasma pretreatment, which indicates an increase in surface reactivity. Since N_2 plasma treated devices showed only marginally improved hysteresis and threshold voltage stability over the Ar plasma, it can be concluded that cleaning the surface (reducing O-C bonds) is the likely dominant factor to improve the interface quality.

Conclusions

We have developed a model to explain the main electrical differences resulting from untreated and plasma pretreated surfaces in MOSHEMTs. Despite the uncertainty in the interface state density and distribution, we have been able to use the DIGS model combined with discrete donors to explain consistently the observed changes in quasi-equilibrium threshold voltage, hysteresis and reverse bias stress resulting from different pre-deposition surface preparations. Our measurements and analysis add further insight into the mechanisms affecting V_{TH} instabilities, but indicate that the elimination of these effects relate to the significant reduction in interface states, which are implicated in the inability to easily achieve E-mode devices.

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