High-Performance MMIC Inductors for GaN-on-Low-Resistivity Silicon for Microwave Applications

A. Eblabla, X. Li, D. J. Wallis, I. Guiney, and K. Elgaid

***Abstract*— Novel MMIC spiral inductors on GaN-on-low-resistivity silicon (LR-Si) substrates ($\sigma < 40\ \Omega \cdot$ cm) are demonstrated with enhanced self-resonance frequency (f_{SRF}) and Q-factor. The developed technology improves inductor performance by suppressing substrate coupling effects using air-bridge technology above benzocyclobutene dielectric as an interface layer on the lossy substrate. A 0.83-nH spiral inductor with peak Q-factor enhancement of 57% ($Q = 22$ at 24 GHz) and maximum f_{SRF} of 59 GHz was achieved because of the extra 5-μm elevation in air. An accurate broad-band model for the fabricated inductors has been developed and verified for further performance analysis up to 40 GHz. The proposed inductors utilize cost-effective, reliable, and MMIC-compatible technology for the realization of high-performance RF GaN-on-LR Si MMIC circuits for millimeter-wave applications.**

***Index Terms*— Benzocyclobutene (BCB), GaN-based high-electron-mobility transistors (HEMTs), high-Q Inductors, low-resistivity silicon substrates, millimeter wave.**

I. Introduction

GaN-BASED devices offer inherent advantages for the realization of power switches operation at high temperature and high power for millimeter-wave applications. For example, an envelope tracking bandwidth of 20 MHz with power device switching frequencies up to 200 MHz has been demonstrated due to the ongoing work on the integration of GaN high-electron-mobility-transistor (HEMT)-based gate drivers, and buck converters on insulating SiC substrates [1]. The potential use of this circuit for 5G applications using GaN on LR Si substrates, where both power and RF GaN devices featured on the same chip, will introduce the additional advantage of low cost and large diameter wafers, compared with high-resistivity Si and SiC technologies.

High-performance on-chip inductors are one of the key passive components in MMIC circuit implementation [2]. However, substrate parasitics are a major factor that would inhibit the realization of high-performance inductors, with high Q-factors and high f_{SRF} especially at higher microwave frequencies [3]. Therefore, overcoming these parasitics in on-chip inductors remains a key challenge when considering GaN-on-LR Si as a substrate for high-power, high-frequency applications.

Efforts have been reported to enhance inductor characteristics at microwave frequencies, including substrate removal and increased substrate resistivity by ion bombardment [4], [5]. However, these techniques are hindered by the additional fabrication processes, and hence increased cost, to a standard MMIC fabrication. Recently, shielded-elevated CPW (SE-CPW) on benzocyclobutene (BCB) technology was presented as an optimum solution to overcome substrate coupling effects associated with the lossy substrate for GaN-on-LR Si technology [6]. Therefore, the integration of SE-CPW to high Q-factor and f_{SRF} inductors using reliable and MMIC compatible technology must be investigated for the realization of successful MMIC circuits.

In this letter, we report on the realization of a cost-effective MMIC-compatible on-chip inductor technology with reduced parasitics using elevated traces on air and a BCB interface layer. Inductors with various inductance values (0.81–4.3 nH) are designed, fabricated, and characterized based on the extracted inductors model. A maximum Q of 22 at 24 GHz along with peak f_{SRF} of 59 GHz was obtained for 0.81-nH inductors. The developed inductor technology is compatible with many III–V technologies up to K-band applications.

II. Device Fabrication

Inductors were fabricated on AlGaN/GaN HEMT layers grown on 1-mm-thick LR p-type Si (111) substrate, as shown in Fig. 1. Epitaxial layers and growth procedure are detailed in [7]. Optical lithography was used for all levels of device definition. As in a standard MMIC process, mesa isolation was initially performed followed by the deposition of a 200-nm Si_3N_4 dielectric layer.

The fabrication process of the proposed MMIC spiral inductors started by spinning a 5-μm-thick BCB film, which was subsequently fully cured at 250 °C in a N_2 atmosphere. A BCB thickness of 5 μm was chosen, as greater dielectric thicknesses involve difficulties in creating via-holes connections through the BCB for device integration, and could cause additional inductance [6]. Next, alignment markers, SE-CPW ground planes, and inductor underpasses were patterned, followed by

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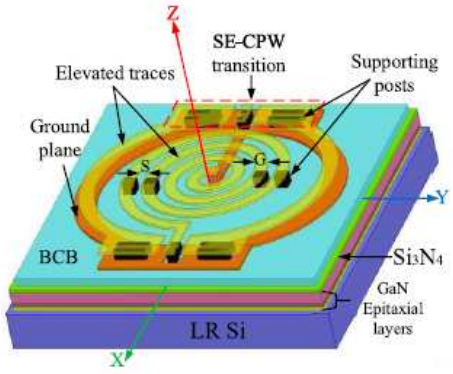

Fig. 1. 3-D view of the fabricated MMIC spiral-elevated inductor integrated to 50-Ω SE-CPW on BCB.

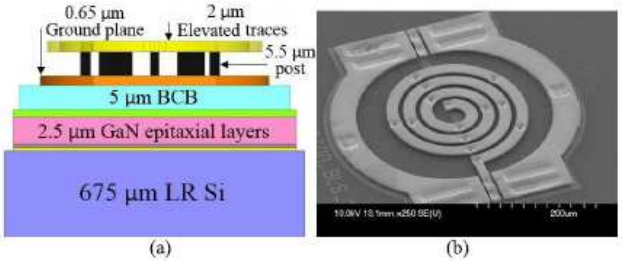

Fig. 2. (a) Cross-sectional view. (b) SEM image of the fabricated elevated inductors.

the metallization and liftoff of a Ti/Au metal stack. Then, the SE-CPW and the inductor-elevated trace loops were achieved using standard air-bridge technology. Finally, the samples were metallized using 2-μm Au electroplating (details of air-bridge fabrication process can be found in [8]). A final elevation high of 5.5 μm was obtained. A cross-sectional view and scanned electron microscopy (SEM) images of the fabricated devices are shown in Fig. 2.

III. Inductor Model

Ansoft HFSS was employed to design the prefabricated devices to ensure best inductor performance. The geometrical parameters corresponding to peak Q-factor and f_{SRF} for all inductor structures are found to be as follows: width $(W) = 19$ μm, spacing $(S) = 25$ μm, and an inner diameter of 38 μm.

For better understanding of inductors' performance/loss mechanisms, an equivalent circuit model is required, especially at high frequencies (i.e., beyond the X-band). The proposed model (shown in Fig. 3) was extracted based on the measured S-parameters. The topology of this model is similar to that proposed in [5], where L_{Prime} is the inductance, R represents the series resistance due to conductor loses, and R_S and L_S are the resistance and inductance associated with skin depth, respectively. C_p represents the capacitive coupling between the spiral turns and the underpass and between two adjacent spiral tracks. C_{d1} and C_{d2} represent the total capacitance between the spirals and conductive Si substrate (including both BCB and

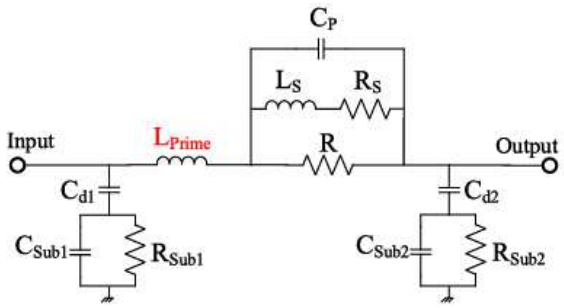

Fig. 3. Schematic of the proposed equivalent circuit model of the fabricated elevated inductors.

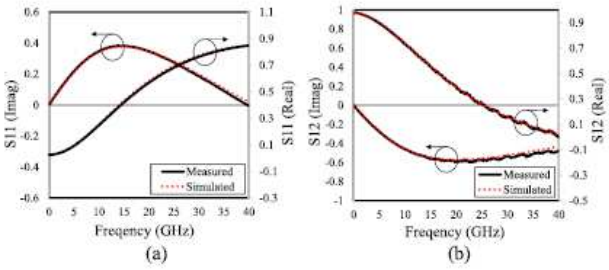

Fig. 4. Measured versus modeled (a) S11 and (b) S21 for a 3-turn spiral-elevated inductor on BCB.

air dielectrics in series), and R_{sub} and C_{sub} are the substrate parameters. The circuit model was verified by the excellent agreement between modeled and measured S-parameters up to 40 GHz, as shown in Fig. 4.

IV. Measurement Results

On-wafer measurements of small-signal S-parameters were performed from 0.1 to 67 GHz. The system was calibrated to the probe tips using off-wafer line-reflect-reflect-match calibration. The measured S-parameters were then converted to Y-parameters, which were subsequently used to calculate the inductance and Q-factor of the fabricated devices [9].

To show the challenges involved in the design of high-performance inductors using SE-CPW technology, three different inductor technologies were realized: shielded-elevated inductors where ground planes were patterned on BCB underneath the elevated spiral loops, inductors fabricated directly on the BCB, and elevated inductors on BCB.

As shown in Fig 5, for the 3-turn inductors, the shielded-elevated inductor achieved the lowest performance, where a Q-factor of as poor as 4 at 17 GHz along with an f_{SRF} of 34 GHz were measured. This could be because the conductive ground plane allows an image current to flow and the negative mutual coupling between the spiral plane and the ground plane reduces the inductance [10]. Using the patterned ground shield instead of solid ground shield can improve inductor performance, but it is limited to lower frequency range [11]. Q-factor and f_{SRF} were further improved to 15 at 23 and 55 GHz, respectively, when fabricating the inductors directly on the BCB. Having the spiral loops elevated in air

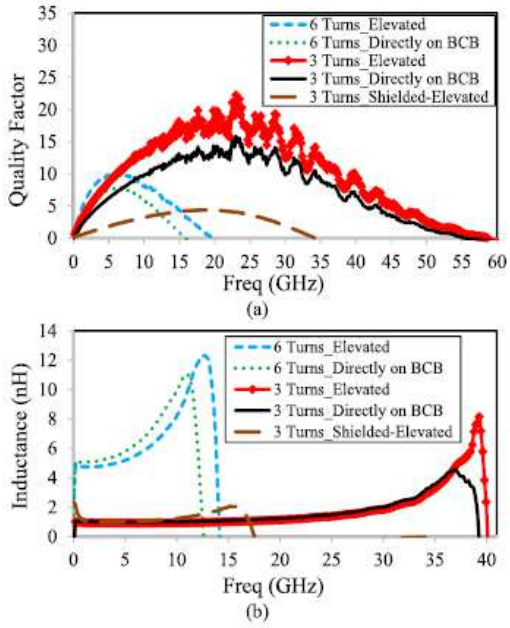

Fig. 5. Comparison of the measured results of the fabricated MMIC inductors versus frequency. (a) Quality-factor. (b) Inductance.

TABLE I

EXTRACTED PARAMETERS FOR THE EQUIVALENT CIRCUIT IN FIG. 2 AND MEASURED Q-FACTOR AND f_{SRF} OF THE INDUCTORS

Parameter	N = 3	N = 4	N = 5	N = 6
L_{Prime} (nH)	0.815	1.517	2.677	4.304
L_s (nH)	0.104	0.464	0.689	1.19
R_s (Ω)	3.73	7.53	9.6	12.5
R (Ω)	7.5	9.1	11.58	16.28
C_{d1} (fF)	18	19.5	24.7	30.06
C_{d2} (fF)	18.8	20.82	26.02	31.26
C_P (fF)	2	3.4	6.8	14.4
R_{sub1}/R_{sub2} (KΩ)	15.8 / 13.3			
C_{sub1}/C_{sub2} (fF)	2			
f_{SRF} (GHz)	59	42	28	15
Q-Factor (Peak)	22	18	15	10

increased the Q-factor by 57% ($Q = 22$ at 24 GHz and $f_{SRF} = 59$ GHz) due to reduced substrate parasitics. However, inductors achieved lower performance at frequencies below X-band due to a finite conductor thickness of 2 μm, where conductor losses are dominant [6]. This could be enormously improved by having thicker conductor metals (by increasing electroplating time during fabrication process). However, at higher frequency range, improvement to inductor performance by increasing the physical conductor thickness is limited by the saturation of the series resistance [12]. Therefore, this technique will not be effective in the millimeter-frequency range.

To further investigate the performance/loss mechanism of the best performing elevated inductors on BCB, inductors with various turns ($N = 3$, 4, 5, and 6) were fabricated and modeled. The model parameters (indicated in Table I) are determined using the S-parameters fitting technique. As shown in Table I, increasing N results in an increase in self-inductance due to the addition of the new conductors, and corresponding increase in the total mutual inductance of the device, resulting in the increase of the inductance value (L_{Prime}). However, as the inductor periphery increases, C_{d1} and C_{d2} and R will be dramatically increased, resulting in degradation of the Q-factor and f_{SRF} [as shown in the results of the 6-turn inductors indicated in Fig. 5(a)].

V. CONCLUSION

High-Q on-chip inductors employing elevated traces and a BCB interface layer have been realized on GaN-on-LR Si to reduce substrate coupling effects. Inductors with inductance varying from 0.81 to 4.3 nH were designed, fabricated, and characterized based on the extracted small-signal model. A peak Q-factor of 22 at 24 GHz and f_{SRF} of 59 GHz was achieved for 0.81-nH inductors. The fabricated MMIC inductors offer a promising technology platform and can be integrated with RF GaN-HEMTs on LR Si for the realization of high-performance MMIC circuits for millimeter-wave applications.

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