

Low-Loss MMICs Viable Transmission Media for GaN-on-Low Resistivity Silicon Technology

A. Eblabla, B. Benakaprasad, X. Li, D. J. Wallis, I. Guiney, and K. Elgaid

Abstract—In this work a novel ultra-low loss transmission media for RF GaN-on-low-resistivity silicon (LR-Si) substrates ($\sigma < 40 \Omega\cdot\text{cm}$) has been successfully demonstrated. The developed shielded-microstrip lines achieve comparable performance to those on semi-insulating (SI) GaAs substrates with transmission loss of 0.9 dB/mm for frequencies up to 67 GHz. Line performance was further enhanced by additional elevation of the shielded-microstrip lines using air-bridge technology above a 5 μm layer of benzocyclobutene (BCB) on shielded metalized ground planes. Transmission loss of 0.6 dB/mm for frequencies up to 67 GHz was obtained as a result of the extra elevation. Structure parameters were designed and optimized based on EM simulation for best performance. The work shows that the RF energy coupled into the substrate was eliminated, indicating the suitability of III-V-on-LR Si technology for millimeter-wave applications.

Index Terms—Benzocyclobutene (BCB), GaN-based HEMTs, low-resistivity silicon substrates, microstrip lines, millimeter-wave.

I. INTRODUCTION

GaN-based high-electron-mobility transistors (HEMT) have outstanding material properties, which enable power-switching operation at high voltages/currents at high speed and efficiency, and with microwave capability that could be utilized in many telecommunications applications. Recent work on the integration of GaN HEMT based gate drivers and buck converters on insulating SiC substrates has achieved envelope tracking bandwidths of 20 MHz with power device switching frequencies up to 200 MHz [1]. The potential use of this circuit for 5G applications using GaN on Si substrates where both Power and RF GaN on the same chip will offer the additional benefit of significantly lower cost. GaN HEMT's grown on LR Si offers the advantage of cost-effective and large diameter wafers which make manufacturing costs of GaN-on-LR Si potentially lower than high-resistivity (HR) Si and SiC technologies.

Low-loss transmission media is a key requirement for the realization of high-quality interconnects and passive elements of the circuit for millimeter-wave applications. However, RF

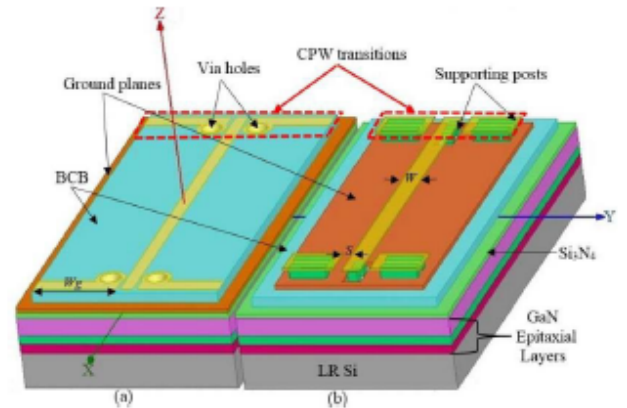


Fig. 1. Oblique projection of the fabricated 1 mm-length 50 Ω lines (a) Shielded-Microstrip line with $S = 4.5 \mu\text{m}$ and $W = 13.2 \mu\text{m}$. (b) Shielded-elevated Microstrip lines with $S = 9 \mu\text{m}$, $W = 20 \mu\text{m}$, $W_g = 100 \mu\text{m}$.

signal coupling to substrate is the main cause of performance degradation when considering LR Si as a substrate. Therefore, substrate loss suppression is a crucial step towards the industrialization of novel GaN on LR Si technology.

Recently, shielded-elevated CPW (SE-CPW) fabricated on GaN-on-LR Si has been developed to reduce the effect of the conductive substrate, achieving a lower attenuation constant compared to that of CPW on SI substrates [2]. Insertion of a low-losses, low dielectric constant, k , layer of BCB as an insulator was proved to be another technique for substrate coupling reduction [3]. This approach, compared to other more complicated techniques [4] [5], has the advantage of accommodating active circuits underneath the passive components and interconnectors with no degradation of active device performance [6].

In this work, shielded (S)-Microstrip and shielded elevated (SE)-Microstrip lines were introduced for substrate-coupling effect suppression. Two design structures were fabricated on GaN-on-LR Si providing almost complete isolation of the lossy substrate, by employing a ground plane and 5 μm -thick BCB layer. The structure with suspended transmission media tracks provided lower dielectric loss with transmission loss of 0.6 dB/mm at V-band frequencies.

II. EXPERIMENTAL WORK

The study was carried out on AlGaIn/GaN HEMT layer grown on 675 μm thick a LR P-type Si (111) substrate, as shown in Fig. 1. Epitaxial layers and growth procedure are detailed in [7].

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A. Eblabla, B. Benakaprasad, X. Li, and K. Elgaid are with the School of Engineering, The University of Glasgow, (e-mail: Khaled.Elgaidd@glasgow.ac.uk).

D. J. Wallis and I. Guiney are with the Cambridge Centre for GaN, The University of Cambridge.

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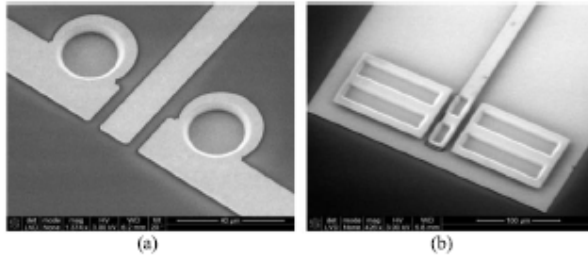


Fig. 2. Scanned Electron Microscopy (SEM) of the fabricated lines. (a) S-Microstrip line and (b) SE-Microstrip line.

All levels of device definition were realized using optical lithography and all steps required to realize the proposed transmission media are compatible with standard MMICs technology. As in a standard MMIC process, two types of Microstrip lines as shown in Fig. 1a) and b) were fabricated simultaneously on the same GaN on LR Si wafer; after mesa isolation and 200 nm Si_3N_4 dielectric layer deposition steps.

The fabrication process of type (a) Microstrip lines, shown in Fig. 1a, started with Ti/Au (50/600 nm) metal deposition to form the markers and ground planes. Then, 5 μm -thick BCB film was spun and fully cured at 250 $^\circ\text{C}$ in an N_2 atmosphere. Next, the CPW-transition's via-holes were defined using AZ4562 resist as a mask prior to CF_4 -based reactive-ion-etching (RIE). Finally, the line tracks were patterned using a standard lift-off process with a Ti/Au (50/600 nm) metal stack. The challenge involved in the developed technology is making the connection between ground and line tracks using standard lithography techniques for MMICs applications.

Type (b) Microstrip lines (illustrated in Fig. 2b) were fabricated in a similar way to type (a); where 5 μm -BCB were initially spun and cured prior to the definition of markers and ground planes levels. Then, air-bridge technology was employed to form the elevated traces' structures including a number of supporting posts. Finally, the sample was metallized using 2 μm gold electroplating.

III. MEASUREMENTS AND MODELLING

On-wafer measurements of small-signal S-parameters were performed using an Agilent PNA network analyzer (E8361A) over the range 0.1-67 GHz. The system was calibrated using line-reflect-reflect-match (LRRM) calibration based on an off-chip ISS impedance standard. 50 μm -pitch Picoprobes were used for probing the CPW-transition parts located at either end of the fabricated Microstrip lines. The samples were placed on a thick quartz spacer to eliminate any possible parasitic substrate modes caused by the metal chuck.

For modelling, a 3-D full-wave electromagnetic simulation tool, Anasoft HFSSTM was employed to design and simulate the prefabricated Microstrip lines. Accurate optimization of the structures was needed (especially for the CPW-transition parts) during the simulation for better performance and to ensure the suppression of RF energy dispersion introduced by the conductive substrate.

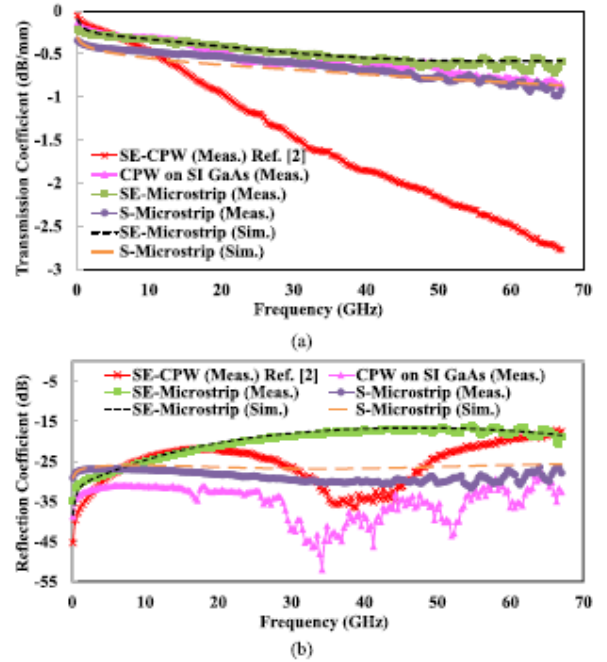


Fig. 3. Measured and simulated S-parameters for the fabricated transmission media. (a) Transmission coefficient (S_{21}). (b) Reflection coefficient (S_{11}).

IV. RESULTS AND DISCUSSION

Fig. 3 shows the RF performance of the developed transmission media for RF GaN-on-LR Si substrates MMIC applications. The performance achieved is comparable with that of traditional CPW on SI substrates and better than that of SE-CPW using air as a spacer on LR Si substrates [2]. Clearly from the measured results, shown in Fig. 3a), the developed technology (S-Microstrip and SE-Microstrip) exhibits an excellent RF performance of transmission loss of 0.9 dB/mm and 0.6 dB/mm at 67 GHz, respectively. Furthermore, the measured results obtained have been verified by the very close agreement between measured and simulated S-parameters. As indicated in Fig. 3a), the proposed, newly developed SE-Microstrip transmission media (shown in Fig. 1b), exhibits the least losses; better than that of the standard CPW on SI substrate and previously developed SE-CPW indicated in [2]. This indicates the almost complete isolation of the conductive substrate, where virtually no conduction current flow, induced current loops or associated losses were allowed through the lossy substrate.

Moreover, it is clearly shown in Fig. 3a) that the effect of the conductive substrate is still noticeable for the SE-CPW lines fabricated on thin Si_3N_4 layer above the lossy substrate. The losses are mainly because the E-field was partially coupled onto the conductive substrate even whilst employing a thin Si_3N_4 insulating layer, which is used to suppress the DC leakage current [8]. This is due to the small areas in the lower ground plane in which the line has physical contact with the lossy substrate.

We believe the developed method using BCB significantly enhances the performance of the transmission line especially

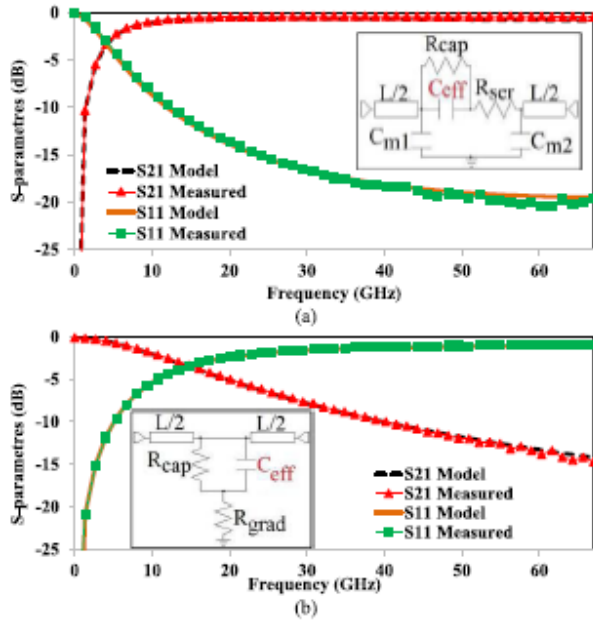


Fig. 4. Measured and modelled S-parameters results and equivalent-circuit-model (Inset) of a $60 \times 20 \mu\text{m}^2$. (a) Series capacitor. (b) Shunt capacitor.

at high frequencies where the gap dimensions of the ground plane at the CPW signal line posts become comparable to the signal wavelength.

In Fig. 3b, a reflection coefficient of always less than -18 dB over the full band shows that the fabricated transmission media were well-matched to a characteristic impedance, Z_0 , of 50Ω . The best matched line was the S-Microstrip line, where a reflection coefficient of less than -29 dB was achieved. This is a clear indication of the high-quality fabrication yield with uniform BCB surface and well-controlled thickness, which determines the Z_0 of the line [9]. Moreover, the resonant frequency was further shifted when BCB was used, indicating the mitigation of undesirable in-band resonances and ensure single-mode propagation for the fabricated Microstrip lines.

To prove the capabilities and efficiency of the developed transmission media, low-loss in-line MIM capacitors, which are a critical part of MMIC circuits design, were realized using S-Microstrip technology. The developed capacitors employ a $200 \text{ nm Si}_3\text{N}_4$ as a dielectric, which has a relative permittivity of approximately 6.7. As shown in Fig. 4, the realized series and shunt capacitors achieved an insertion loss of less than 0.5 dB and 0.8 dB, respectively. This indicates very strong shielding of the lossy substrate.

Advanced Design System (ADS) software was employed for modelling and extraction of the equivalent-circuit-model

TABLE I
DERIVED EQUIVALENT CIRCUIT MODEL AND ITS
COEFFICIENTS FOR 0.45 pF MIM CAPACITORS

Capacitor type	Modelled C_{eff} value (pf)	C_{m1} (pf)	C_{m2} (pf)	R_{ser} (Ω)	R_{cap} (K Ω)
Series	0.4	0.002	0.002	1	>15
	Modelled C_{eff} value (pf)	R_{grad} (Ω)	R_{cap} (K Ω)		
Shunt	0.43	0.12	>15		

element values of the fabricated capacitors (shown in Table I). The circuit model was verified by the excellent agreement between modeled and measured S-parameters over the frequency range, as indicated in Fig. 4.

V. CONCLUSION

In this work, we have developed low-losses Microstrip lines on GaN-on-LR Si. The fabricated lines suppressed substrate loss effects by electromagnetic decoupling of the lossy Si. Consequently, a transmission loss, S_{21} , of 0.6 dB/mm was achieved. These results are even better than those achieved using MMICs conventional transmission media on a standard SI GaAs substrate. The proposed transmission media offers a promising technology for the integration of high RF performance active devices and low-losses high-Q passive elements for the realization of MMIC circuits at mm-wave frequencies.

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